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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,930	03/13/2001	Yochai Parchak	100.005US01	1922

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EXAMINER	
HOANG, THAI D	
ART UNIT	**PAPER NUMBER**
2667	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,930	PARCHAK ET AL.	
	Examiner	Art Unit	
	Thai D Hoang	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Application filed on 03/13/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-14 and 16-20* is/are rejected.

7)☒ Claim(s) *8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/30/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 9, 12, 14, 16, 19-20 are rejected under 35 U.S.C. 102(e) as being unpatentable over Fujisawa et al, US Patent No. 6,785,290 B1, herein after referred to as Fujisawa.

Regarding claims 1, 9, 16 and 20, Fujisawa discloses a line interface integrated circuit and packet switch. In figures 1 and 3, the line card disclosed by Fujisawa show the line interface comprises a physical layer interface 12. The line cards inherently comprise a plurality of input ports, wherein each of the plurality of input ports couples with a physical layer interface 12 for processing ATM cells. In addition, Fujisawa teaches that the line cards classify priority of the incoming cells (class information, CI) into data queues DQ1-DQ5 (fig. 2), which are stored in the buffer 24. Then, the ATM cells are outputted to the switch interface 22 based on the priority of the cells stored in the queues; figs. 1-4, col. 3, line 65-col. 4, line 8, col. 7, lines 3-24, and 48-52 (a plurality of physical layer devices, each of said physical layer devices adapted to support cells of first and second priorities and including a controllable port, said ports in operative

communication with each other to provide for the transmission of all cells of said first priority from all of said plurality of physical layer devices before transmitting any cells of said second priority from all of said plurality of physical layer devices).

Regarding claims 12 and 19, Fujisawa suggest that five data queues DQ1 to DQ5 may correspond to ATM service categories, CBR, rt-BVR, nrt-VBR, UBR and ABR; col. 6, lines 64-67 (wherein determining when any of the physical layer devices has priority traffic in a queue comprises determining when any of the physical layer devices have constant bit rate traffic).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa as shown above.

Regarding claim 2, Fujisawa discloses the line card comprises a cell storage controller 20 for controlling output cells that are stored in the buffer 24. Fujisawa discloses all of the cells in the queues DQ1-DQ5 are stored in the buffer 24. Fujisawa 0does not teach the queues are separately stored in different buffers. However, one of ordinary skill in the art would be able to modify Fujisawa's system by storing each of the queues DQ1-DQ5 in a different buffer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujisawa's line card by

adding buffers, wherein each of the buffers stores only cells having the same priority level in order to queue and dequeue cells easily.

Regarding claim 3, Fujisawa discloses that when the host CPU 26 (state machine) detects that the length of the host queue HQ is 1 or more (counting), it requests the scheduler 16 to dequeue data from the host queue HQ. In this case, the scheduler 16 selects one of queues having a length not smaller than 1 and the highest output priority from the data queues DQ1 to DQ5 and the host queue HQ, and makes it dequeue cells from the buffer 24; col. 7, lines 53-59 (a counter; a state machine; and a buffer operably coupled to said counter and said state machine.)

Regarding claim 4, the ports in the line card Fujisawa are inherently connected along a bus.

Claims 5-7, 10-11 13-14 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa as shown above in view of Chiussi et al, US Patent No. 6,785,290 B1, herein after referred to as Fujisawa and Chiussi respectively.

Regarding claims 5 and 13, Fujisawa discloses a line interface integrated circuit and packet switch. In figures 1 and 3, the line card disclosed by Fujisawa show the line interface comprises a physical layer interface 12. The line cards inherently comprise a plurality of input ports, wherein each of the plurality of input ports couples with a physical layer interface 12 for processing ATM cells. In addition, Fujisawa teaches that the line cards classify priority of the incoming cells (class information, CI) into data queues DQ1-DQ5 (fig. 2), which are stored in the buffer 24. Then, the ATM cells are outputted to the switch interface 22 based on the priority of the cells stored in the

queues; figs. 1-4, col. 3, line 65-col. 4, line 8, col. 7, lines 3-24, and 48-52. The physical layer interfaces are inherently coupled to a bus for processing incoming cells. Fujisawa does not explicitly disclose the physical layer interfaces access to the bus in a round robin fashion. Also, Fujisawa does not disclose a second bus, coupled to the priority status port of each of the physical layer devices, the second bus providing an indication as to whether any of the physical layer devices has cells in its respective first queue to allow for priority handling of cells in the first queue. However, Chiussi discloses the system operates in a round robin fashion, col. 12, lines 29-38. Furthermore, Chiussi discloses that the system transmits ATM cells based on priority status of the bus; col. 15, lines 8-17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply priority status of the bus and Round Robin fashion disclosed by Chiussi into Fujisawa's for advantages cited above with respect to claim 10.

Regarding claim 6, Fujisawa does not explicitly disclose the line cards use UTOPIA standard. However, the UTOPIA standard is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply UTOPIA standard into Fujisawa's system in order to adapt with conventional system used in the network.

Regarding claim 7, Fujisawa suggest that five data queues DQ1 to DQ5 may correspond to ATM service categories, CBR, rt-BVR, nrt-VBR, UBR and ABR; col. 6, lines 64-67 (wherein the physical layer devices each have a high priority queue for constant bit rate traffic and a low priority queue for non-constant bit rate traffic.)

Regarding claims 10-11 and 17-18, Fujisawa discloses that the cells are transmitted based on priority level. However, Fujisawa does not explicitly disclose the cells are transmitted in a Round Robin fashion. However, Chiussi discloses a system in which ATM cells are transmitted in a Round Robin fashion. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Round Robin fashion into Fujisawa's in order to improve the quality of service because the cells delivered based on theirs priority.

Regarding claim 14, Fujisawa suggest that five data queues DQ1 to DQ5 may correspond to ATM service categories, CBR, rt-BVR, nrt-VBR, UBR and ABR; col. 6, lines 64-67 (wherein determining when any of the physical layer devices has priority traffic in a queue comprises determining when any of the physical layer devices have constant bit rate traffic).

Allowable Subject Matter

Claim 8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to the application:

US Patent No. 6,147,997 A, Holden et al discloses "Mechanism to support an UTOPIA interface over a backplane"

US Patent No. 5,889,778 A, Huscroft et al discloses "ATM layer device"

US Patent Application Publication 2001/0030974 A1, Pauwels discloses "Switch and a switching method"

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai D Hoang whose telephone number is (571) 272-3184. The examiner can normally be reached on Monday-Friday 10:00am-18:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Hoang

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER

11/10/04